What is claimed is:

1. A semiconductor integrated circuit device having a memory cell array in which nonvolatile semiconductor memory devices are arranged in a matrix with a plurality of rows and columns,

wherein each of the nonvolatile semiconductor memory devices comprises:

a word gate formed on a semiconductor layer with a first gate insulating layer interposed;

an impurity diffusion layer which forms either a source region or a drain region; and

first and second control gates in the shape of sidewalls formed along either side of the word gate, wherein:

the first control gate is disposed on the semiconductor layer with a second gate insulating layer interposed, and also on the word gate with a side insulating layer interposed;

the second control gate is disposed on the semiconductor layer with another second gate insulating layer interposed, and also on the word gate with another side insulating layer interposed;

the first and second control gates extend in a first direction; and

a pair of the first and second control gates, adjacent in a second direction which intersects the first direction, is connected to a common contact section.

2. The semiconductor integrated circuit device as defined

in claim 1,

wherein each of the first and second control gates is formed of a conductive layer extending in the direction in which the impurity diffusion layer extends.

3. The semiconductor integrated circuit device as defined in claim 1,

wherein the common contact section is connected to the first and second control gates and includes a conductive layer formed of the same material as the first and second control gates.

4. The semiconductor integrated circuit device as defined in claim 1,

wherein the common contact section includes an insulating layer formed on the semiconductor layer, a conductive layer formed on the insulating layer, and a cap layer formed on the conductive layer.

5. The semiconductor integrated circuit device as defined in claim 4,

wherein the insulating layer is formed of a laminate consisting of a first silicon oxide layer, a silicon nitride layer, and a second silicon oxide layer.

6. The semiconductor integrated circuit device as defined in claim 1, wherein:

the side insulating layers are located between the word gate and the first and second control gates; and

the upper ends of the side insulating layers are located higher than the first and second control gates with respect to the semiconductor layer.

7. The semiconductor integrated circuit device as defined in claim 1, wherein:

the buried insulating layer is formed between the two side insulating layers disposed in contact with the first and second control gates; and

the buried insulating layer covers the adjacent first and second control gates.

8. The semiconductor integrated circuit device as defined in claim 1,

wherein the common contact section is provided in contact with one end of the impurity diffusion layer.

9. The semiconductor integrated circuit device as defined in claim 1,

wherein the common contact sections are staggered relative to each other.

10. The semiconductor integrated circuit device as defined in claim 1, wherein:

the memory cell array is divided into a plurality of

blocks; and

the impurity diffusion layers in blocks adjacent to each other in the first direction are connected to each other through a contact impurity diffusion layer formed in the semiconductor layer.

11. The semiconductor integrated circuit device as defined in claim 1,

wherein the second gate insulating layer is formed of a laminate consisting of a first silicon oxide layer, a silicon nitride layer, and a second silicon oxide layer.

12. The semiconductor integrated circuit device as defined in claim 1,

wherein the side insulating layer is formed of a first silicon oxide layer, a silicon nitride layer, and a second silicon oxide layer.

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